Fully Depleted Silicon-on-Insulator (FDSOI) CMOS Technology Optimized for Enhanced Geothermal System Temperature Operation

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Keywords

Fully Depleted Silicon-on-Insulator, FDSOI, Complementary Metal Oxide Semiconductor, CMOS, High-Temperature Electronics, Enhanced Geothermal Electronics, Extreme Environment Electronics

ABSTRACT

This paper describes a Fully Depleted Silicon-on-Insulator (FDSOI) Complementary Metal Oxide Semiconductor (CMOS) technology capable of operating at 300°C. With its near-ideal subthreshold swing, and greatly reduced semiconductor cross-sectional junction area as compared to both bulk and Partially Depleted Silicon-on-Insulator (PDSOI) technologies, the FDSOI transistor structure represents the optimal high-temperature silicon-based device, making it an ideal, cost-effective candidate to fabricate both complex digital and mixed-signal circuits for enhanced geothermal applications.

1. Introduction

Enhanced geothermal energy production requires electronic systems capable of executing measurement, monitoring and control tasks at temperatures in excess of 250° C [1]. Several semiconductor material systems and integrated circuit process technologies are being considered to fulfill this electronics need including, wide band-gap materials like silicon carbide (SiC) and gallium nitride (GaN), along with more conventional narrow band-gap silicon technologies. Both SiC and GaN-based electronics have shown excellent high temperature operation [2,3]; however, these processes are less mature, higher cost, and lower speed than traditional silicon-

based electronics. In addition, the complexity of the integrated circuits (ICs) that have been demonstrated in these material systems has been limited to a few hundred transistors in GaN [4], and a few thousand transistors in SiC [5]. In contrast, silicon-based electronics, utilizing Complementary Metal Oxide Semiconductor (CMOS) technology, make up the backbone of the modern microelectronics industry and are used in nearly every computer, smart phone and sensor system in use today. These mature silicon-based technologies have been used to reliably mass-produce ICs with billions of transistors [6]. Traditionally the operation of these silicon-based electronic systems, even in military systems, have been limited to temperatures ≤125° C [7] making them unsuitable for enhanced geothermal applications. The principle limiter on the high-temperature performance of traditional silicon CMOS is the increase in parasitic leakage currents associated with the reverse-bias semiconductor junctions in the transistor structure. As a rule-of-thumb these leakage currents double for every 10° C increase in temperature. One of the keys to enhancing the high temperature performance of silicon transistors is to minimize the semiconductor junction cross-sectional area in the device structure. Using a Partially Depleted Silicon-on-Insulator (PDSOI) CMOS technology variant, which greatly reduces the transistor semiconductor junction area, commercial ICs capable of operating at 225° C have been demonstrated and are available on the market [8,9]. This paper describes a Fully Depleted Silicon-on-Insulator (FDSOI) CMOS technology capable of operating at 300° C. With its near-ideal subthreshold swing[1], and further reduced junction area, as compared to PDSOI, the FDSOI device structure represents the ultimate high-temperature silicon-based transistor, making it a strong candidate to fabricate both complex digital and mixed-signal circuits for enhanced geothermal applications.

2. Bulk vs Partially and Fully Depleted Silicon-on-Insulator Technology

As CMOS technologies continue to scale, fully depleted device concepts (ultra-thin-body SOI, finFET, and others) have been displacing traditional bulk CMOS technologies [10, 11]. The ultra-thin fully depleted body of the transistor allows for tighter electrostatic control of the transistor channel resulting in better short-channel-performance than can be achieved with the traditional bulk CMOS device structure. Figure 1 shows schematic cross-sections of both a silicon-on-insulator (SOI) CMOS and a traditional bulk CMOS device structure. Devices in the SOI process are fully oxide isolated from one another, unlike in the bulk process where reversed biased silicon diodes are used in conjunction with either a shallow trench or field oxide isolation. The full oxide isolation of the SOI structure (both partially depleted, and fully depleted) allows greater device packing densities and greatly reduced (>100x) semiconductor diode junction areas. This significantly reduces the parasitic capacitances of the device structure leading to lower power and/or higher performance device operation. In addition, the greatly reduced semiconductor junction area in the SOI device significantly decreases the temperature-induced parasitic leakage currents in the device enhancing the high temperature performance of the SOI transistor. These benefits are further improved with the ultra-thin-body FDSOI structure which reduces the source/drain-to-body junction areas by an additional 2-5x, as compared to PDSOI,

[1] Subthreshold Swing is a measure of how quickly a transistor turns on when voltage is applied to the gate of the device. For a bulk or partial depleted (PDSOI) transistor at room temperature the subthreshold swing is a decade increase in transistor drive current for every ~80-90mV applied to the transistor gate. For a fully depleted (FDSOI) transistor the room temperature subthreshold swing is ~65-70mV/decade.

and also reduces the transistor channel depletion capacitances resulting in a near-ideal transistor subthreshold swing of ~65-70mV/decade of drive current at room temperature. This near-ideal subthreshold swing of the FDSOI transistor structure translates into an additional ~70° C increase in the operational temperature limits of the transistor when compared to a PDSOI device with a subthreshold swing of 85-90mV/decade of drive current at room temperature.

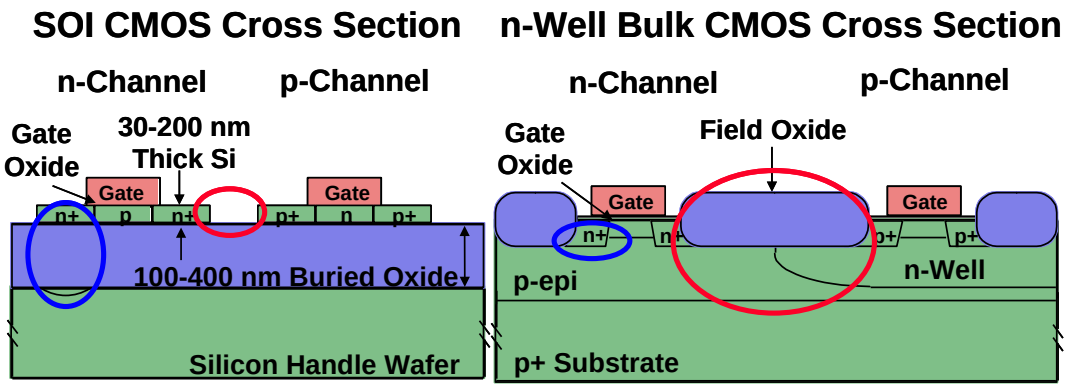

Figure 1. Schematic cross-sectional drawings of SOI CMOS (left) and an n-well bulk CMOS (right) technologies. For a PDSOI device the thin top silicon layer is ~70-200 nm thick. For FDSOI the top silicon layer is <50 nm thick.

3. Experiment

Using both MIT Lincoln Laboratory's (MIT-LL) 90-nm, 1.2V FDSOI CMOS technology and 180-nm, 1.5V technology, test devices and circuits were fabricated and characterized at elevated temperature. The principal features of the FDSOI CMOS technology are a 150-nm buried oxide (BOX) thickness on a high-resistivity float zone substrate, 30-nm thick SOI device layer thickness, ultra-shallow trench isolation, 1.8-nm gate oxide, dual-doped polysilicon gates, oxide/nitride spacers, cobalt salicide, seven-levels of aluminum-based interconnect with planarized dielectrics, and tungsten plug contacts and via connections. All features are defined using a 193-nm ASML scanner with a 26 × 32-mm field of view. The baseline 90-nm technology has an unloaded inverter delay of ~15ps/stage at 1.2 V; f_T for the n- and p-FETs are 115 and 50 GHz, respectively. The process incorporates dual-threshold voltage transistors, Vt_1 = ±400mV and Vt_2 = ±600mV at room temperature. High temperature testing was performed using the 600mV Vt_2 devices. In addition to a full range of transistor sizes, transistor topologies, and process monitors, the principal circuit used in the evaluation was a 2's complement static multiplier circuit. This simple 4,000 transistor screening circuit is a standard process monitor used in all FDSOI CMOS fabrication lots at MIT-LL.

Figure 2 shows a cross-sectional transmission electron micrograph (TEM) of a completed 90-nm FDSOI transistor. In this process technology each individual transistor is fully isolated from its neighbors using a silicon dioxide insulating layer, and utilizes an active silicon transistor layer that is 30-nm thick. The only diode junction area in this device susceptible to high-temperature-

induced leakage currents are the source and drain contacts to channel junctions highlighted by the blue dashed lines in the TEM. This FDSOI junction area is >100x lower than would be found in a comparably sized bulk CMOS technology and ~2-5x lower than in a comparably sized PDSOI technology.

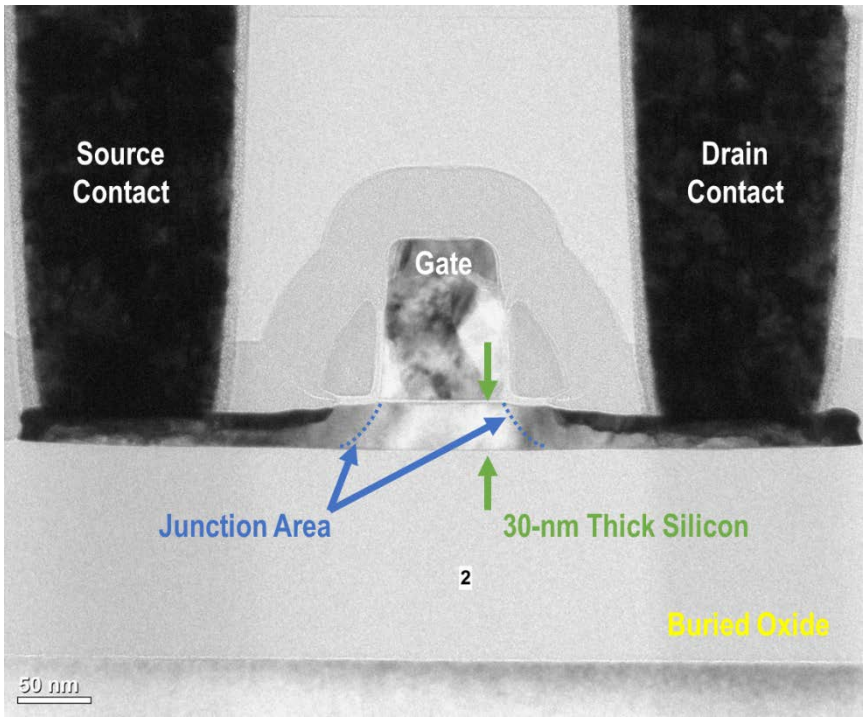

Figure 2. Cross-sectional Transmission Electron Micrograph (TEM) of a completed 90-nm Fully Depleted Silicon-on-Insulator (FDSOI) CMOS transistor optimized for extreme environments.

4. Results

Figure 3 is the transistor drain current vs gate voltage plots for both a p-channel (left) and an n-channel (right) FDSOI device operated at a drain bias of 1.5V volts (worst case bias for thermally induced leakage current). As the temperature of the device is increased from room temperature 21° C (blue data points) to 300° C (red data points) the transistor threshold voltage decreases (transition point from the subthreshold region to the saturation region moves closer to zero volts), the subthreshold swing degrades (slope of the curves in the subthreshold region gets lower), the ON-state (Gate Voltage =±1.5 volts) drive current decreases, and the OFF-state (Gate Voltage = 0 volts) leakage current increases. All of these changes are detrimental to successful device and circuit operation. To minimize the impact of transistor OFF-state leakage current with increasing temperature on circuit performance it is necessary to minimize the baseline room temperature leakage current of the device. For the FDSOI transistor this is accomplished by starting with a high-threshold-voltage transistor design which coupled with the near ideal subthreshold swing (steeper starting slope in the subthreshold region) results in a low room temperature OFF-state leakage current. Since the FDSOI process technology offers both low

and high threshold voltage transistors, the higher ±600mV threshold devices were used for the high temperature transistor and circuit measurements. These higher threshold transistors help reduce the impact of the exponential increase of the off-state leakage current with increased temperature at the expense of a small reduction in transistor's ON-state drive current. As shown in the data, even at 300° C, there is still approximately a three-orders-of-magnitude difference between the "ON" and "OFF" state currents for these transistors, more than enough to allow for successful operation of digital circuits at this elevated temperature.

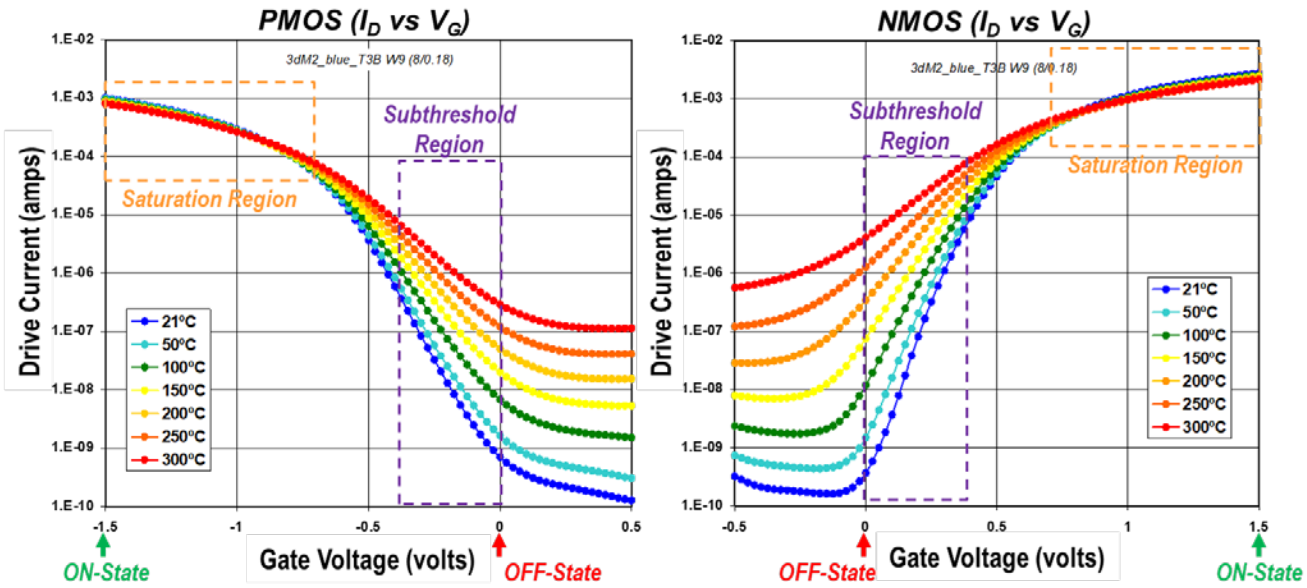

Figure 3. Semi log plots of transistor drive current (ID) vs gate voltage (VG) for the ±600mV threshold voltage FDSOI p-channel (left) and n-channel (right) transistors, with the drain voltage (VD=1.5V), and increasing temperature 21° C to 300° C as the parameter. The subthreshold and saturation regions of the transistor operation are also shown.

Figure 4 shows the clock period time vs power supply voltage shmoo plots[2] for the multiplier circuit operating from room temperature 300K (27° C) through 573K (300° C). Note that the functional space (green region) for the circuit decreases up until ~200° C and then remains reasonably constant up to the measured maximum of 300° C. Even at 300° C a large fully functional operational window exists for this circuit.

[2] A shmoo plot is a graphical display of the response of an electronic component or system varying over a range of conditions or inputs

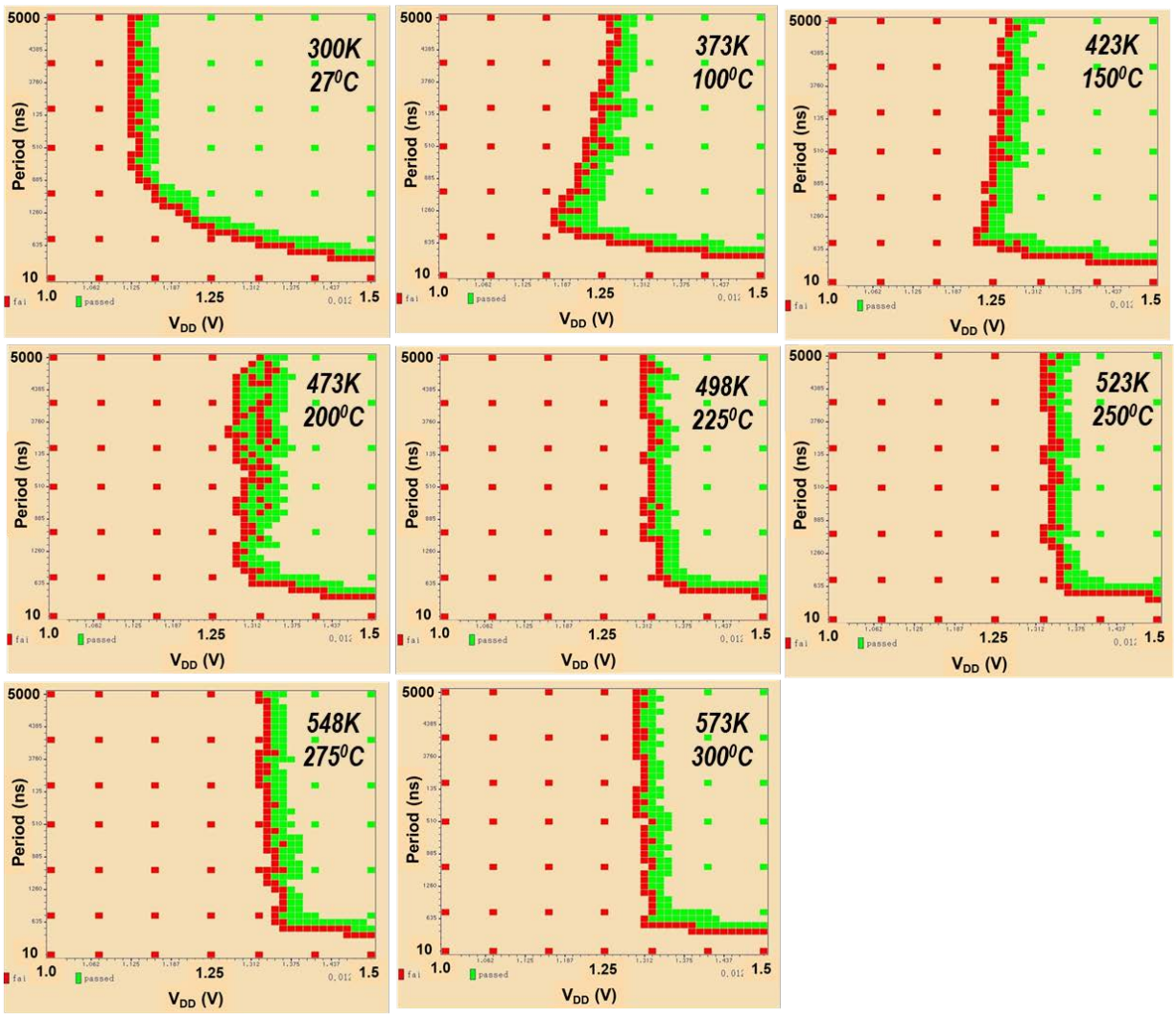

Figure 8. Clock period time vs power supply voltage shmoo plots for the multiplier circuit operating from room temperature 300K (27° C) through 573K (300° C).

5. Conclusion

The full oxide device isolation, near-ideal subthreshold swing, reduced parasitic capacitances, and greatly reduced junction area of FDSOI make it an ideal silicon-based technology for use in a broad range of extreme environment applications. An insulating oxide provides dielectric isolation between devices. At higher temperatures, thermally induced junction leakage current is minimized due to the greatly reduced junction area in a FDSOI device allowing circuits to operate at 300° C. The 90-nm version of the existing MIT Lincoln Laboratory 90-nm FDSOI CMOS technology is currently being transferred to the Skywater Technology Foundry in Bloomington, MN, which is offering an Early Access Partner Program.[3] This technology

[3] https://www.skywatertechnology.com/rad-hard-eap/

transfer will allow the extreme environments circuit design community *(including the Enhanced Geothermal Community)* to leverage this unique process for both complex digital and mixed-signal circuits necessary for their applications.

Acknowledgement

This work was sponsored by DARPA, DTRA, and the DoD under contract numbers FA8721-05-C-0002, FA8702-15-D-0001, and NASA JPL under IAA. Opinions, interpretations, conclusions, and recommendations are those of the authors and are not necessarily endorsed by the United States Government.

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